Accelerator Development Department
RHIC Project
Brookhaven National Laboratory
Associated Universities, Inc.
Upton, New York 11973

Specification for the RHIC Real Time Data Link Transmitter System

October 27, 1993

H. Hartmann

Note: for SNS, an 8 bit CRC checkword was added to replace the parity bit. The output of the V105S is a differential ECL signal level. All register assignments are identical.

Rev. 0.0 09-29-92
Rev 1.0 10-30-92
Rev 2.0 12-07-92
Rev 3.0 04-09-93
Rev 3.1 08-06-93
Rev. 4.0 10-27-93
Rev. 4.1 01-27-94

1.0 Introduction

This document describes a system that makes available to all locations around the RHIC ring certain machine parameters of general interest to users. The system is modeled after the FermiLab MDAT System whereby specific parameters of the accelerator are broadcast to all users. This RHIC Real Time Data Link consists of frames of serial data broadcast over a single cable. Each frame has the following format:

*1 start bit
*8 bit parameter ID field
*24 bit parameter field
*1 parity bit
*1 stop bit.

Each frame will be encoded as a 10Mbit Bi-Phase Mark signal. A signal transition always occurs at the beginning of the 100ns bit cell, and a transition within the cell indicates a "1" while no transition indicates a "0". Each frame is transmitted at a rate that coincides with the 720 Hz RCLK event, and is 3.5us duration.

RHIC Real Time Data Link Frame Protocol

|---|
| 0 | MSB-Parameter ID - LSB | MSB -Parameter Data - LSB | P | 1 |

Each group of frames will consist of, but not be limited to, the following parameters:

1. Programmed Blue Ring Current
2. Programmed Blue Ring Current Dot
3. Measured Blue Ring Current
4. Measured Blue Ring Current Dot
5. Programmed Yellow Ring Current
6. Programmed Yellow Ring Current Dot
7. Measured Yellow Ring Current
8. Measured Yellow Ring Current Dot

It also may be desirable to have a number of frames that contain beam intensity for each of the RHIC rings, as well as time of day.

Eight (8) RHIC Real Time Data Link parameters are currently defined (out of a possible 255), and sufficient time exists to transmit all possible 255 events. A 10 MHz carrier will be transmitted between data frames, and each frame will be time domain multiplexed onto the RHIC Real Time Data Link. This scheme of transmission is the same as the Event Line currently being used in the AGS/Booster Timing system, and therefore can take advantage of existing fan-out and repeater circuits.

The RHIC Real Time Data Link Transmitter System consists of two boards: an input board and an encoder board. The encoder board will be a single board whose inputs are from the dual channel input boards.

2.0 RHIC Real Time Data Link Data Input Board

2.1 Functionality

Each channel on this dual channel board consists of a set of registers which interface to the device and another set of registers which interface to the VME bus. Each channel is identified by its parameter ID. The Device Data Register holds the most recent parameter loaded from the device and is loaded via a fiber optic serial bi-phase mark encoded link. Update timing of the Device Data Register is controlled by the device. The VME Data Register holds a 24 bit parameter that is downloaded from the VME bus Master. Update timing of the VME Data Register is controlled by the VME bus timing. Both the Device Data Register and the VME Data Register can be read by the VME bus Master. Depending on the mode, data is strobed from either the Device Data Register or the VME Data Register into the output register synchronous with the 720 Hz clock event. When loading of the output register is complete, the Input Board will be polled by the Encoder board and, depending on the mode, the appropriate data will be transfered to the Encoder board's output shift register.

Additionally, there shall be 64 address locations resident in prom that will hold Status/ID information about the board. This Status/ID information can be read by the VME bus Master. (See page 4)

The parameter id is determined by a set of user configurable jumper blocks located on the board.

2.2 Modes of Operation

1.) VME Mode. RHIC Real Time Data Link parameter values are downloaded from the VME Master for transmission on the RHIC Real Time Data Link.

2.) Device Mode. RHIC Real Time Data Link parameter values are loaded from the device for transmission on the RHIC Real Time Data Link. The parameter loaded from the device is from a serial data link. This data is encoded as a bi-phase mark encoded bit stream and has the same protocol as the RHIC Real Time Data Link Frame.

2.3 Hardware Architecture

2.3.1 System Bus

The Input Board is a VME slave with a variety of registers whereby command and status information can be accessed. This board will respond to address modifier codes for supervisory and non-privileged short (A16) I/O access (29H, 2DH). This board will occupy a 256-byte contiguous block of I/O address space on the VME backplane. The base address is user configurable by a set of jumper blocks, and can be located on any 256-byte boundary within the 64k byte I/O address space. A 16 bit data bus (D16) shall be implemented to return all data structures and this board supports D16, D08(EO) and D08(O) Data Bus Transfer cycles. BLOCK TRANSFER (BLT) and Read-Modify-Write (RMW) bus cycles are not permitted. This Slave will also decode the DS0*, DS1*, LWORD*, IACK*, and A01 control lines. VME

handshake protocol lines such as DTACK*, WRITE*, and AS* will also be supported. Generation of a BERR* signal on the VME bus will not be implemented .

2.3.2 I/O Interface

2.3.2.1 Outputs

The Output of the Input Board will be via a local 24 bit parallel data bus. All outputs (other than the commands and status from the VME bus Master) will go to the Encoder board. Data transfer is accomplished via a handshaking mechanism that is initiated by the Encoder Board.

2.3.2.1 Inputs

Data is input via a fiber optic serial data link which loads the parameter to be broadcast.

2.4 VME bus Master (Front End Computer) to Input Board Communication Protocol

2.4.1 Status/ID Prom

Located at the Base Address is the Input Board Identification Prom. It contains 32 words of 16 bit status/ID information pertaining to the board. Each of the odd bytes is defined below, and each of the even bytes contains an ascii period (.). This data is read only by the VME bus Master.

Offset from Board Base Address	Value Ascii Character	Value Numeric	Description
01H	V	56H	Always VMEID
03H	M	4DH	
05H	E	45H	
07H	I	49H	
09H	D	44H	
0BH	B	42H	Manufacturer I.D. : BNL
0DH	N	4EH	
0FH	L	4CH	
11H	alpha	V	Alpha-numeric board description
13H	numeric	1	
15H	numeric	0	

17H	numeric	6	
19H	reserved		
1BH	reserved		
1DH	reserved		
1FH	reserved		
21H	rev - MSD		Major Rev Level
23H	rev - LSD		2-digit alphabetic
25H	rev - MSD		Minor Rev Level
27H	rev - LSD		2-digit numeric
29H	SN - MSD		Board Serial Number
2BH	SN		4-digit decimal numeric
2DH	SN		
2FH	SN - LSD		
31H	unassigned		Reserved
33H	unassigned		
35H	unassigned		
37H	unassigned		
39H	unassigned		
3BH	unassigned		
3DH	unassigned		
3FH	unassigned		

2.4.2 VME Master communication ports per channel

Located at the base address + 64 is the 16 bit command register. Writing to this register will set the configuration of the board. Reading from this register will provide information about the current command state. The VME Data Register will reside at the BASE ADDR + 68 address location. Writing to this location will set the current VME Data, however, this data will not be loaded into the Encoder Board's output shift register unless the VME Data Enable Command is true. Reading from this location will access the current VME Data Register value. The Device Data Register will reside at the BASE ADDR + 72 address location. This is a read only register and returns the current device data. Since the VME Data Register and the Device Data Register are both 24-bit registers, and the VME data bus is only 16 bits, two bus cycles are required to access these registers. Located at BASE ADDR + 86 is the Status/ Interrupt Status Register. This is a read only register and returns the current status of the serial link and the interrupt statuses.

Resident as part of the slave is the RORA (Release On Register Access) interrupter. The interrupt level is set in the command register. The contents of the Interrupt Vector Register are automatically placed on the VME data bus during the interrupt acknowledge cycle. Interrupt statuses will be cleared after reading the Status/Interrupt Status Register. Both Status/Interrupt Status Registers must be read to determine the cause of the interrupt.

a. One 16-bit command register, read/write
b. One 16- bit status/interrupt status register, read only
c. One 24-bit VME Data register, read/write
d. One 24-bit Device Data register,read only

2.4.2.1 Register Configuration

Address	Description
Base Addr + 64 (40H)	Command Register CH1
Base Addr + 66 (42H)	Command Register CH2
Base Addr + 68 (44H)	VME Data Register CH1 (15-0)
Base Addr + 70 (46H)	VME Data Register CH1 (23-16)
Base Addr + 72 (48H)	VME Data Register CH2 (15-0)
Base Addr + 74 (4AH)	VME Data Register CH2 (23-16)
Base Addr + 76 (4CH)	Device Data Register CH1 (15-0)
Base Addr + 78 (4EH)	Device Data Register CH1 (23-16)
Base Addr + 80 (50H)	Device Data Register CH2 (15-0)
Base Addr + 82 (52H)	Device Data Register CH2 (23-16)
Base Addr + 84 (54H)	Interrupt Vector Register (7-0)
Base Addr + 86 (56H)	Status/Interrupt Status Register CH1 (15-0)
Base Addr + 88 (58H)	Status/Interrupt Status Register CH2 (15-0)
.	.
.	.
.	.
Base Addr + 255 (FFH)	End of Register Space

2.4.2.2 Bit assignments of the registers:

Command Register:
bit 0 ===> Reset
bit 1 ===> Mode (VME/Device)
bit 2 ===> Halt/Load (VME Data)
bit 3 ===> Interrupt Enable
bit 4 ===> Go
bit 5-7 ===> INTerrupt CoDe (1..3)
bit 8-15 ===> Undefined

Status register:
bit 0 ===> Link Status
bit 1 ===> CRC Error Status
bit 2 ===> Frame Error Status
bit 3 ===> Link Interrupt Status
bit 4 ===> CRC Interrupt Status
bit 5 ===> Frame Interrupt Status

bit 6-7 ===> Undefined
bit 8-15 ===> Parameter ID

Interrupt Vector Register: bit 7-0 ===> Vector #

2.4.2.2.1 Command Bits:

RESET. When SET, '1',all latched commands will be cleared.

VME Data ENABLE/DISABLE. When SET, '1', VME data will be loaded into the Encoder Board's output shift register. When CLEARED, '0', the device data will be loaded into the Encoder Board's output shift register.

HALT/LOAD VME Data. When SET, '1', this will allow the processor to load all bytes into the VME Data Register before new VME data is sent to the encoder board. This bit must be CLEARED, '0', before new VME data will be sent to the encoder board. This bit is only relevant if MODE is SET. (VME Data)

Interrupt Enable. When SET, '1', interrupts will be generated on the VMEbus. The Status/Interrupt Status Registers should be read to clear any pending interrupts before asserting Interrupt Enable. When CLEARED, '0', interrupts will not be generated on the VMEbus. Interrupt statuses are valid regardless of the the state of the Interrupt Enable Bit.

Go. When SET, '1', data will be allowed to pass to the Encoder Board. When CLEARED, '0', Board needs to be initialized.

INTCD(1..3). Interrupt Level (7-0). This is the Interrupt Level that the board will generate on the VMEbus when the Interrupt Enable bit is set.

On Power-Up, all command bits are CLEARED. The Power-Up Default Configuration is as follows:

NOT RESET
MODE-Device
LOAD VME Data.
Interrupts Disabled.
NOT Go
INTCD(1..3) ==> 000

2.4.2.2.2 Status Bits:

The following bits are either set or cleared based on the functionality of the board, and cannot be user controlled:

Link Status. This bit is SET, '1', when the carrier on the local serial link has been properly detected. This bit will be CLEARED, '0', when the carrier has not been detected for 2us (10 clock cycles).

CRC Error Status. This bit is SET, '1', when a frame has been received with a data integrity error. This bit is CLEARED, '0', when a frame with no data errors has been received.

Frame Error Status. This bit is SET, '1', when a frame start has been detected but no frame end. This bit is CLEARED, '0', when the next valid frame has been received.

Link Interrupt Status. This bit is SET, '1', when the carrier on the local serial link has not been detected for 2us. This bit is CLEARED, '0', when the Status/Interrupt Status Register is read.

CRC Interrupt Status. This bit is SET, '1', when a CRC Error has been detected. This bit is CLEARED, '0', when the Status/Interrupt Status Register is read.

Frame Interrupt Status. This bit is SET, '1', when a Frame Error has been detected. This bit is CLEARED, '0', when the Status/Interrupt Status Register is read.

Parameter ID. Jumper configurable.

2.5 Electrical Specification

All register and id prom address decoding will be accomplished via PAL PLD devices.

Voltages: +5V @ 2.5A

2.6 Physical Specification

This board will consist of two distinct channels with one VME Interface and will be resident on a 6U, 160mm standard VME size B board. It will occupy a standard 4HP chassis space.

Front panel indicators will include CH1 SERLNK, CH1 Error, CH2 SERLNK, CH2 Error and VME SEL.

Front panel inputs will consist of two ST-type fiber optic connectors for the local serial link.

3.0 RHIC Real Time Data Link Encoder Board

3.1 Functionality

RHIC Real Time Data Link frames will be time domain multiplexed onto the RHIC Real Time Data Link via the Encoder Board, by servicing each of the Input Boards individually until all RHIC Real Time Data Link frames have been transmitted. RHIC Real Time Data Link events appear on the link in the order in which they are defined in the encoder board. The parameter ID identifies the particular frame and not the placement of the frame in time relative to another frame. The transmission sequence for all defined parameter id codes is synchronous with the 720 Hz clock event, and therefore, this board will incorporate a timeline decoder circuit as well as an event decoder circuit.

3.2 Hardware Architecture

3.2.1 System Bus

The Encoder Board is a VME slave with a variety of registers whereby command and status information can be accessed. This board will respond to address modifier codes for supervisory and non-privileged short (A16) I/O access (29H, 2DH). This board will occupy a 512-byte contiguous block of I/O address space on the VME backplane. The base address is user configurable by a set of jumper blocks, and can be located on any 512-byte block boundary within the 64k byte I/O address space. A 16 bit data bus (D16) shall be implemented to return all data structures. BLOCK TRANSFER (BLT) and Read-Modify-Write (RMW) bus cycles are not permitted. This Slave will also decode the DS0*, DS1*, LWORD*, IACK*, and A01 control lines. VME handshake protocol lines such as BERR*, DTACK*, WRITE*, and AS* will also be supported. The Encoder Board has the provision of generating a jumper selectable interrupt. An interrupt can be generated by the loss of the RHIC Event Line carrier or by the non response, when polled, of any input channel.

Additionally, there shall be 64 address locations resident in prom that will hold Status/ID information about the board. This Status/ID information can be read by the VME bus Master.
(See page10)

3.2.2 I/O Interface

3.2.2.1 Outputs

The only output from this board is the RHIC Real Time Data Link pulse train. This signal consists of a unipolar TTL signal comprised of a finite number of individual frames that are time domain multiplexed and coupled to the link via a RS422 differential driver with 100 ohm characteristic impedance.

3.2.2.2 Inputs

Inputs to this board will be via a local 32 bit parallel data bus from the Input Board. Polling of each Input Board and handshaking protocols between boards are controlled by the Encoder Board.

3.3 VME Master to Encoder Board Communication Protocol

3.3.1 Status/ID Prom

Located at the Base Address is the Encoder Board Identification Prom. It contains 32 words of 16 bit status/ID information pertaining to the board. Each of the odd bytes is defined below, and each of the even bytes contains an ascii period (.). This data is read only by the VME bus Master and can be accessed by D16, D08(EO) and D08(O) Data Bus Transfer cycles.

Offset from Board Base Address	Value Ascii Character	Value Numeric	Description
01H	V	56H	Always VMEID
03H	M	4DH	
05H	E	45H	
07H	I	49H	
09H	D	44H	
0BH	B	42H	Manufacturer I.D. : BNL
0DH	N	4EH	
0FH	L	4CH	
11H	alpha	V	Alpha-numeric board description
13H	numeric	1	
15H	numeric	0	
17H	numeric	5	
19H	reserved		
1BH	reserved		
1DH	reserved		
1FH	reserved		
21H	rev - MSD		Major Rev Level
23H	rev - LSD		2-digit alphabetic
25H	rev - MSD		Minor Rev Level
27H	rev - LSD		2-digit numeric
29H	SN - MSD		Board Serial Number
2BH	SN		4-digit decimal numeric
2DH	SN		

2FH	SN - LSD	
31H	unassigned	Reserved
33H	unassigned	
35H	unassigned	
37H	unassigned	
39H	unassigned	
3BH	unassigned	
3DH	unassigned	
3FH	unassigned	

3.3.2 VME Master Communication Ports

Located at the base address + 64 is the 16 bit command register. Writing to this register will set commands. Reading from this register will provide information about the current command state. Located at base addreess + 66 is the Status Register. This register is read only and holds board configuration, timing, and error information. The interrupt vector register is a read/write register located at the base addr + 68. All registers can be accessed by the VMEbus Master by D16, D08(EO), and D08(O) Data Bus Transfer cycles.

Resident as part of the slave is the RORA (Release On Register Access) interrupter. The interrupt level is set in the command register. The contents of the Interrupt Vector Register are automatically placed on the VME data bus during the interrupt acknowledge cycle. Interrupt statuses will be cleared after reading the Status Register.

a. One 16-bit command register, read/write
b. One 16- bit status register, read only
c. One 16- bit interrupt vector register, read/write bit 0-7 are significant.

3.3.2.1 Register Configuration

Address	Description
Base Addr + 64 (40H)	Command Register
Base Addr + 66 (42H)	Status Register
Base Addr + 68 (44H)	Interrupt Vector Register (7-0)
.	.
.	.
.	.
Base Addr + 255 (FFH)	End of Register Space

3.3.2.2 Bit assignments of the registers:

Command Register:
bit 0 ===> Reset
bit 1 ===> External Trigger On/Off
bit 2 ===> Go ; Init Done/not done
bit 3 ===> Interrupt Enable/Disable

bit 4 ===> Undefined
bit 5-7===> INTCD(1..3)
bit8-15===> Undefined

Status Register:
bit 0 ===> NO REPly ERRor
bit 1 ===> INITDONE/ERROR
bit 2 ===> RCLKACT
bit 3 ===> 720Hz Active
bit 4 ===> RTDLACT Transmitter Active
bit 5 ===> NOREPINT No REPly INTerrupt
bit 6 ===> RCLKINT RCLK INTerrupt
bit 7 ===> Undefined
bit 8-15 ===> IDCODE(0..7) (only important if NoReply Error)

Interrupt Vector Register: bit 7-0 ===> Vector #

3.3.2.2.1 Command Bits:

RESET. When SET, '1', all latched commands will be cleared and the current frame data transmission will be terminated.

External Trigger ON. When SET, '1', the loading of data into the output shift register will be dependent on a user supplied external trigger. When CLEARED, '0', the loading of data into the output shift register will be dependent on a decoded Rhic Event, by default, the 720Hz Event.

GO. When SET, '1', this signifies that the Parameter ID Codes list has been downloaded from the FEC.

Interrupt Enable. When SET, '1', interrupts will be generated on the IRQx line selected. When CLEARED, '0', interrupts will not be generated. Error conditions can be determined by reading the status register.

INTCD(1..3). Interrupt Level (7-0). This is the Interrupt Level that the board will generate on the VMEbus when the Interrupt Enable bit is set.

On Power-Up, all command bits are CLEARED. The Power-Up Default Configuration is as follows:

not RESET
External Trigger OFF
Initialize NOTDONE
Interrupts DISABLED

3.3.2.2.2 Status Bits:

The following bits are either set or cleared based on the functionality of the board, and cannot be user controlled:

NO REPly ERRor. This bit is SET on the first occurrence of a non-response from any channel of the Input Board. If every input channel on the Input Board responds when polled, this bit will be automatically CLEARED.

INITDONE/ERROR. This bit is SET on the first occurrence of a 00H Parameter ID Code. This bit is CLEARED if the Parameter ID Code list contains no End-of List Code. (00H)

RCLKACT - RHIC Event Line Active. This bit is SET when a carrier is detected on the RHIC Event Line. This bit is CLEARED when no RHIC Event Line carrier has been detected for 1us. (10 clock cycles)

720ACT - 720 Hz Event Active. This bit is SET when the 720Hz event has been decoded. This bit is CLEARED when no 720Hz event has been decoded for 5ms. (4 trigger cycles)

RTDLACT - Transmitter (Encoder) Active. This bit is SET when a carrier is detected on the RHIC Real TimeData Line. This bit is CLEARED when no RTDL carrier has been detected for 1us. (10 clock cycles)

NOREPINT. NO REPly INTerrupt Status. This bit is SET, '1', when a particular ID Code has not responded when polled. This bit is CLEARED, '0', when the Status Register is read.

RCLKINT. RCLK INTerrupt Status. This bit is SET, '1', when no RHIC Event Line carrier has been detected for 1us. This bit is CLEARED, '0', when the Status Register is read.

IDCODE(0..7) - Parameter ID Code. These bits indicate the Parameter ID Code of the first input that does not respond. These are only valid when NOREPERR is SET.

3.3.3 Parameter ID Codes SRAM

Located at the base address + 256 is a 256 x 8-bit volatile read/write memory. Immediately after Power-Up, the VMEbus Master (FEC) must write to this SRAM the Parameter ID Codes list. After this list has been properly downloaded, the GO bit in the command register must be SET. These are the valid Parameter ID codes that will appear on the RTDL. Once an initial list has been loaded, a Parameter ID Code can be added and will appear on the RTDL during the next trigger cycle. Parameter ID Codes can be deleted as well. This memory is shared by the FEC and the encoder sequencer, with priority going to the encoder sequencer. VMEbus access to this memory is granted or delayed relative to the state of the encoder sequencer. VMEbus accesses are allowed whenever the encoder sequencer doesn't require data from the SRAM. This SRAM only supports D08(EO) and D08(O) Data Bus Transfer cycles. A BERR* will be generated for any other Data Bus Transfer cycle.

Address	Contents
Base Addr + 256 (100H)	Parameter ID Code #1
Base Addr + 257 (101H)	Parameter ID Code #2
Base Addr + 258 (102H)	Parameter ID Code #3
.	.

.	.
.	.
Base Addr + (256 + n)	Parameter ID Code #n
Base Addr + (256 + n + 1)	00H
.	.
.	.
Base Addr + 511 (1FFH)	End of RAM Space

3.4 Electrical Specification

All register and id prom address decoding as well as command decoding will be accomplished via PAL PLD devices.

Clock decoding will be accomplished via an Altera EPM5032 gate array and will be compatible with the existing AGS/Booster Timeline.

The encoding section will be resident in a gate array. The polling addresses of the Input Boards will reside in volatile memory. Should any Input Board not respond when polled, an error will be generated and the VME Master will be notified via an interrupt. An interrupt will also be generated to signify a loss of the RHIC Event Line carrier. Bussed across the backplane will be the LDDATA signal, which is derived from the 720 Hz clock event, and loads the VME Data Register or the Device Data register into the output register located on the Input Board.

Voltages: +5V @ 2.5A

3.5 Physical Specification

This board will consist of one VME Interface section, a generic RHIC Event Line decoder circuit, and the RHIC Real Time Data Link encoder section all of which will be resident on a 6U, 160mm standard VME size B board. It will occupy a standard 4Hp chassis space.

Front panel indicators will include RTDL ACTive, 720 Hz ACTive, LOAD ACTive, EventLink and VME SEL.

EventLink Input will be from a front panel twinax connector. RHIC Real Time Data Link info will be available at both the backplane and via a twinax connector on the front panel. An external BNC trigger input will available on the front panel.

Buffered RHIC Event line and RHIC Real Time Data Link will be available via front panel BNC connectors.

References:

1.) 0812-ED-35678 ACCELERATOR CONTROLS CAMAC 166-
MDAT TRANSMITTER SCHEMATIC 3-6-85

2.) D36-E449-5 REVC VME TIMING SYSTEM DECODER
SCHEMATIC 10/4/90

3.) 0812-ED-218512 ACCELERATOR CONTROLS CAMAC C465
POWER SUPPLY INTERFACE
SCHEMATIC 11/8/89

4.) CONTROLS HARDWARE RELEASE NO. 45.3
"CAMAC 166 MODULE - MDAT TRANSMITTER"
R. J. DUCAR 8/25/88

5.) AGS TECHNICAL NOTE
"FIBER OPTICS GENERAL INTERFACE"
R. MARIOTTI 6/23/89

6.) THE VMEbus SPECIFICATION REV C.1 9/85